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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/836,449	04/17/2001	Stephen J. Fonash	823.0052USQ1	7746

22204 7590 06/07/2004

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EXAMINER	
BOOTH, RICHARD A	

ART UNIT	PAPER NUMBER
2812	

DATE MAILED: 06/07/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/836,449	FONASH ET AL.	
	Examin r	Art Unit	
	Richard A. Booth	2812	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *22 March 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-99* is/are pending in the application.

4a) Of the above claim(s) *98 and 99* is/are withdrawn from consideration.

5)☒ Claim(s) *73-96* is/are allowed.

6)☒ Claim(s) *1-21,24-28 and 34-72* is/are rejected.

7)☒ Claim(s) *22-23 and 29-33* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *3/12/02*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Election/Restrictions

Applicant's election of the electronics species is acknowledged. Because applicant did not distinctly and specifically point out the supposed errors in the restriction requirement, the election has been treated as an election without traverse (MPEP § 818.03(a)).

Request for Information

Under 37 CFR 1.105, the examiner requests information in the form of publications, patents, etc. to which applicant may be aware regarding columnar void network morphology formation (see MPEP 704.10).

Claim Objections

Claims 22-23 are objected to under 37 CFR 1.75(c) as being in improper form because a multiple dependent claim must be in the alternative when referring to more than one claim. See MPEP § 608.01(n). Accordingly, the claims 22-23 have not been further treated on the merits.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

Claims 1-2 and 10-12 are rejected under 35 U.S.C. 102(b) as being anticipated by Guilinger et al., U.S. Patent 4,995,954.

Guilinger et al. shows the invention as claimed including a method of processing a substrate comprising the steps of: forming a high surface area to volume ratio material layer (porous silicon) over a surface of a substrate; and removing at least a portion of said porous silicon layer (see col. 2-line 30 to col. 3-line 58).

Regarding claim 2, note that the ratio of the porous silicon will inherently have a ratio of up to 10,000 to 1.

Concerning claims 10-12, note that the removal of the porous silicon layer is through wet etching (see col. 3-lines 49-52).

Claims 1-2, 10-12, 14-17, 21, 34, 37, 41-46, 50, 57, 64, 66, 69, and 72 are rejected under 35 U.S.C. 102(b) as being anticipated by Xiang-Zheng et al., U.S. Patent 5,242,863.

Xiang-Zheng et al. shows the invention as claimed including a method of processing a substrate 10 comprising the steps of: forming a high surface area to volume ratio material layer (porous silicon) 32 over a surface of a substrate; and removing at least a portion of said porous silicon layer (see col. 6-line 62 to col. 8-line 15 and figs. 3A-3K).

Regarding claim 2, note that the ratio of the porous silicon will inherently have a ratio of up to 10,000 to 1.

Concerning claims 10-12, note that the removal of the porous silicon layer is through wet etching (see col.7-lines 59-61).

With respect to claims 14-17 and 21, note the additional coating (18,36,46) over the porous silicon.

Concerning claim 34, note that a material system 18 is deposited on said substrate 10 prior to step (a), followed by selectively removing portions of said deposited system retaining a portion of said materials system.

Regarding claims 41-42, note that the substrate 10 is silicon.

Claims 1-2, 10-11, 14-16, 21, 34-37, 41-46, 50, 57, 61, 64, 66, and 72 are rejected under 35 U.S.C. 102(b) as being anticipated by Steiner et al., "Using porous silicon as a sacrificial layer".

Steiner et al. shows the invention as claimed including shows the invention as claimed including a method of processing a substrate comprising the steps of: forming a high surface area to volume ratio material layer (porous silicon) over a surface of a substrate; and removing at least a portion of said porous silicon layer (see fig. 2 and its description).

Regarding claim 2, note that the ratio of the porous silicon will inherently have a ratio of up to 10,000 to 1.

Concerning claims 10-11, note that the removal of the porous silicon layer is through etching.

With respect to claims 14-16 and 21, note the additional coating over the porous silicon (see introduction).

Concerning claim 34, note that a material system is deposited on said substrate prior to step (a), followed by selectively removing portions of said deposited system retaining a portion of said materials system.

Regarding claims 41-42, note that the substrate is silicon.

Claims 1-2, 10-12, 14-17, 21-22, 37, 41-45, and 50-53 are rejected under 35 U.S.C. 102(b) as being anticipated by Yonehara et al., "ELTRAN; SOI-Epi Wafer by Epitaxial Layer Transfer from Porous Si".

Yonehara et al. shows the invention as claimed including a method of processing a substrate comprising the steps of: forming a high surface area to volume ratio material layer (porous silicon) over a surface of a substrate; and removing at least a portion of said porous silicon layer (see fig. 1 and its description).

Regarding claim 2, note that the ratio of the porous silicon will inherently have a ratio of up to 10,000 to 1.

Concerning claims 10-12, note that the removal of the porous silicon layer is through etching.

With respect to claims 14-17 and 21-22, note the additional coatings over the porous silicon.

Regarding claims 41-42, note that the substrate is silicon.

Claims 1-2, 10-12, 14-16, 18, 20, 21, 34, 37, 41-50, 57, 61, 64, 66, 68, and 72 are rejected under 35 U.S.C. 102(b) as being anticipated by Tu et al., U.S. Patent 5,352,635.

Tu et al. shows the invention as claimed including a method of processing a substrate 10 comprising the steps of: forming a high surface area to volume ratio material layer (porous silicon) over a surface of a substrate; and removing at least a portion of said porous silicon layer (see fig. 3A-3I and their description).

Regarding claim 2, note that the ratio of the porous silicon will inherently have a ratio of up to 10,000 to 1.

Concerning claims 10-12, note that the removal of the porous silicon layer is through etching.

With respect to claims 14-16, 20-21, and 47, note the additional coatings over the porous silicon and the through-holes formed through the overlying layers (see figs. 3E-3G).

Concerning claim 34, note that a material system is deposited on said substrate prior to step (a), followed by selectively removing portions of said deposited system retaining a portion of said materials system.

Regarding claims 41-42, note that the substrate is silicon.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

This application currently names joint inventors. In considering patentability of the claims under 35 U.S.C. 103(a), the examiner presumes that the subject matter of the various claims was commonly owned at the time any inventions covered therein were made absent any evidence to the contrary. Applicant is advised of the obligation under 37 CFR 1.56 to point out the inventor and invention dates of each claim that was not commonly owned at the time a later invention was made in order for the examiner to consider the applicability of 35 U.S.C. 103(c) and potential 35 U.S.C. 102(e), (f) or (g) prior art under 35 U.S.C. 103(a).

Claims 3-8, 38-40, and 58-60 are rejected under 35 U.S.C. 103(a) as being unpatentable over Tu et al., U.S. Patent 5,352,635 in view of Kalkan et al., "Nanocrystalline Si thin films with arrayed void-column network deposited by high density plasma" or Robbie et al., U.S. Patent 6,248,422.

Tu et al. is applied as above but fails to expressly disclose where the porous layer is a columnar void deposited layer.

Kalkan et al. discloses the formation of a columnar void deposited layer (see abstract). In view of this disclosure, it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify the process of Tu et al. so as to form the porous layer of a columnar void deposited layer as disclosed by Kalkan et al. because these layers have a very high porosity while enjoying the unique properties of

conventional porous layers. Alternatively, Robbie et al. discloses the formation of a columnar void deposited layer (see fig. 6 and its description). In view of this disclosure, it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify the process of Tu et al. so as to form the porous layer of a columnar void deposited layer as disclosed by Robbie et al. because these layers can be made to have an excellent porosity and are suitable as porous layers (see, for example, col. 2-lines 14-20).

Regarding the particular processing parameters of the columnar layer, it would have been obvious to one of ordinary skill in the art to determine through routine experimentation the optimum processing parameters and would not lend patentability to the instant application absent the showing of unexpected results.

Claims 3-8, 38-40, and 58-60 are rejected under 35 U.S.C. 103(a) as being unpatentable over Yonehara et al., "ELTRAN; SOI-Epi Wafer by Epitaxial Layer Transfer from Porous Si". in view of Kalkan et al., "Nanocrystalline Si thin films with arrayed void-column network deposited by high density plasma" or Robbie et al., U.S. Patent 6,248,422.

Yonehara et al. is applied as above but fails to expressly disclose where the porous layer is a columnar void deposited layer.

Kalkan et al. discloses the formation of a columnar void deposited layer (see abstract). In view of this disclosure, it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify the process of Yonehara et al. so

as to form the porous layer of a columnar void deposited layer as disclosed by Kalkan et al. because these layers have a very high porosity while enjoying the unique properties of conventional porous layers. Alternatively, Robbie et al. discloses the formation of a columnar void deposited layer (see fig. 6 and its description). In view of this disclosure, it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify the process of Yonehara et al. so as to form the porous layer of a columnar void deposited layer as disclosed by Robbie et al. because these layers can be made to have an excellent porosity and are suitable as porous layers (see, for example, col. 2-lines 14-20).

Regarding the particular processing parameters of the columnar layer, it would have been obvious to one of ordinary skill in the art to determine through routine experimentation the optimum processing parameters and would not lend patentability to the instant application absent the showing of unexpected results.

Claims 3-8, 38-40, and 58-60 are rejected under 35 U.S.C. 103(a) as being unpatentable over Tu et al., U.S. Patent 5,352,635 in view of Kalkan et al., "Nanocrystalline Si thin films with arrayed void-column network deposited by high density plasma" or Robbie et al., U.S. Patent 6,248,422.

Tu et al. is applied as above but fails to expressly disclose where the porous layer is a columnar void deposited layer.

Kalkan et al. discloses the formation of a columnar void deposited layer (see abstract). In view of this disclosure, it would have been obvious to one of ordinary skill

in the art at the time the invention was made to modify the process of Tu et al. so as to form the porous layer of a columnar void deposited layer as disclosed by Kalkan et al. because these layers have a very high porosity while enjoying the unique properties of conventional porous layers. Alternatively, Robbie et al. discloses the formation of a columnar void deposited layer (see fig. 6 and its description). In view of this disclosure, it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify the process of Tu et al. so as to form the porous layer of a columnar void deposited layer as disclosed by Robbie et al. because these layers can be made to have an excellent porosity and are suitable as porous layers (see, for example, col. 2-lines 14-20).

Regarding the particular processing parameters of the columnar layer, it would have been obvious to one of ordinary skill in the art to determine through routine experimentation the optimum processing parameters and would not lend patentability to the instant application absent the showing of unexpected results.

Claims 3-8, 38-40, and 58-60 are rejected under 35 U.S.C. 103(a) as being unpatentable over Steiner et al., "Using porous silicon as a sacrificial layer" in view of Kalkan et al., "Nanocrystalline Si thin films with arrayed void-column network deposited by high density plasma" or Robbie et al., U.S. Patent 6,248,422.

Steiner et al. is applied as above but fails to expressly disclose where the porous layer is a columnar void deposited layer.

Kalkan et al. discloses the formation of a columnar void deposited layer (see abstract). In view of this disclosure, it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify the process of Steiner et al. so as to form the porous layer of a columnar void deposited layer as disclosed by Kalkan et al. because these layers have a very high porosity while enjoying the unique properties of conventional porous layers. Alternatively, Robbie et al. discloses the formation of a columnar void deposited layer (see fig. 6 and its description). In view of this disclosure, it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify the process of Steiner et al. so as to form the porous layer of a columnar void deposited layer as disclosed by Robbie et al. because these layers can be made to have an excellent porosity and are suitable as porous layers (see, for example, col. 2-lines 14-20).

Regarding the particular processing parameters of the columnar layer, it would have been obvious to one of ordinary skill in the art to determine through routine experimentation the optimum processing parameters and would not lend patentability to the instant application absent the showing of unexpected results.

Claims 3-8, 38-40, and 58-60 are rejected under 35 U.S.C. 103(a) as being unpatentable over Xiang-Zheng et al., U.S. Patent 5,242,863 in view of Kalkan et al., "Nanocrystalline Si thin films with arrayed void-column network deposited by high density plasma" or Robbie et al., U.S. Patent 6,248,422.

Xiang-Zheng et al. is applied as above but fails to expressly disclose where the porous layer is a columnar void deposited layer.

Kalkan et al. discloses the formation of a columnar void deposited layer (see abstract). In view of this disclosure, it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify the process of Xiang-Zheng et al. so as to form the porous layer of a columnar void deposited layer as disclosed by Kalkan et al. because these layers have a very high porosity while enjoying the unique properties of conventional porous layers. Alternatively, Robbie et al. discloses the formation of a columnar void deposited layer (see fig. 6 and its description). In view of this disclosure, it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify the process of Xiang-Zheng et al. so as to form the porous layer of a columnar void deposited layer as disclosed by Robbie et al. because these layers can be made to have an excellent porosity and are suitable as porous layers (see, for example, col. 2-lines 14-20).

Regarding the particular processing parameters of the columnar layer, it would have been obvious to one of ordinary skill in the art to determine through routine experimentation the optimum processing parameters and would not lend patentability to the instant application absent the showing of unexpected results.

Claims 3-8 are rejected under 35 U.S.C. 103(a) as being unpatentable over Guilinger et al., U.S. Patent 4,995,954 in view of Kalkan et al., "Nanocrystalline Si thin

films with arrayed void-column network deposited by high density plasma" or Robbie et al., U.S. Patent 6,248,422.

Guilinger et al. is applied as above but fails to expressly disclose where the porous layer is a columnar void deposited layer.

Kalkan et al. discloses the formation of a columnar void deposited layer (see abstract). In view of this disclosure, it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify the process of Guilinger et al. so as to form the porous layer of a columnar void deposited layer as disclosed by Kalkan et al. because these layers have a very high porosity while enjoying the unique properties of conventional porous layers. Alternatively, Robbie et al. discloses the formation of a columnar void deposited layer (see fig. 6 and its description). In view of this disclosure, it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify the process of Guilinger et al. so as to form the porous layer of a columnar void deposited layer as disclosed by Robbie et al. because these layers can be made to have an excellent porosity and are suitable as porous layers (see, for example, col. 2-lines 14-20).

Regarding the particular processing parameters of the columnar layer, it would have been obvious to one of ordinary skill in the art to determine through routine experimentation the optimum processing parameters and would not lend patentability to the instant application absent the showing of unexpected results.

Claims 54-56 are rejected under 35 U.S.C. 103(a) as being unpatentable over Yonehara et al., "ELTRAN; SOI-Epi Wafer by Epitaxial Layer Transfer from Porous Si" in view of Tayanaka et al., "Thin-Film Crystalline Silicon Solar Cells Obtained by Separation of a Porous Silicon Sacrificial Layer".

Yonehara et al. is applied as above but fails to expressly disclose bonding to a second organic substrate. Tayanaka et al. discloses forming a solar cell using wafer bonding to a second organic plastic substrate (see abstract and fig. 1, for example). In view of this disclosure, it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify the process of Yonehara et al. so as to use a second plastic substrate in the wafer bonding process because this leads to a large cost savings.

Claims 9, 13, 24-27, 62-63, and 65 are rejected under 35 U.S.C. 103(a) as being unpatentable over Tu et al., U.S. Patent 5,352,635 in view of Welbourn et al., U.S. Patent 5,262,000.

Tu et al. shows the invention as claimed but fails to expressly disclose wherein the porous layer is formed upon an intervening layer located between the porous layer and the substrate, wherein a portion of the intervening layers is removed, selectively etching so as to retain a portion of a sacrificial layer,

Welbourn et al. discloses a method of using sacrificial layers S1 and S2, whereby a portion of the sacrificial layers is retained, an intervening layer is located between the sacrificial layer S2 and the substrate S, the sacrificial layer S2 is patterned, wherein

removal of the sacrificial layer S2 removes a portion of the underlying sacrificial layer S1, and wherein through holes are opened to reach the sacrificial layer followed by the formation of additional layers to close the through holes (see figs. 1-12 and their description). In view of this disclosure, it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify the process of Tu et al. so as to use the sacrificial layer process of Welbourn et al. so as to form a MEMS device because this is shown to be a suitable method in which to form a MEMS device.

Claims 9, 13, 24-27, 62-63, and 65 are rejected under 35 U.S.C. 103(a) as being unpatentable over Yonehara et al., "ELTRAN; SOI-Epi Wafer by Epitaxial Layer Transfer from Porous Si" in view of Welbourn et al., U.S. Patent 5,262,000.

Yonehara et al. shows the invention as claimed but fails to expressly disclose wherein the porous layer is formed upon an intervening layer located between the porous layer and the substrate, wherein a portion of the intervening layers is removed, selectively etching so as to retain a portion of a sacrificial layer,

Welbourn et al. discloses a method of using sacrificial layers S1 and S2, whereby a portion of the sacrificial layers is retained, an intervening layer is located between the sacrificial layer S2 and the substrate S, the sacrificial layer S2 is patterned, wherein removal of the sacrificial layer S2 removes a portion of the underlying sacrificial layer S1, and wherein through holes are opened to reach the sacrificial layer followed by the formation of additional layers to close the through holes (see figs. 1-12 and their description). In view of this disclosure, it would have been obvious to one of ordinary

skill in the art at the time the invention was made to modify the process of Yonehara et al. so as to use the sacrificial layer process of Welbourn et al. so as to form a MEMS device because this is shown to be a suitable method in which to form a MEMS device.

Claims 9, 13, 24-27, 62-63, and 65 are rejected under 35 U.S.C. 103(a) as being unpatentable over Steiner et al., "Using porous silicon as a sacrificial layer" in view of Welbourn et al., U.S. Patent 5,262,000.

Steiner et al. shows the invention as claimed but fails to expressly disclose wherein the porous layer is formed upon an intervening layer located between the porous layer and the substrate, wherein a portion of the intervening layers is removed, selectively etching so as to retain a portion of a sacrificial layer,

Welbourn et al. discloses a method of using sacrificial layers S1 and S2, whereby a portion of the sacrificial layers is retained, an intervening layer is located between the sacrificial layer S2 and the substrate S, the sacrificial layer S2 is patterned, wherein removal of the sacrificial layer S2 removes a portion of the underlying sacrificial layer S1, and wherein through holes are opened to reach the sacrificial layer followed by the formation of additional layers to close the through holes (see figs. 1-12 and their description). In view of this disclosure, it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify the process of Steiner et al. so as to use the sacrificial layer process of Welbourn et al. so as to form a MEMS device because this is shown to be a suitable method in which to form a MEMS device.

Claims 9, 13, 24-27, 62-63, and 65 are rejected under 35 U.S.C. 103(a) as being unpatentable over Xiang-Zheng et al., U.S. Patent 5,242,863 in view of Welbourn et al., U.S. Patent 5,262,000.

Xiang-Zheng et al. shows the invention as claimed but fails to expressly disclose wherein the porous layer is formed upon an intervening layer located between the porous layer and the substrate, wherein a portion of the intervening layers is removed, selectively etching so as to retain a portion of a sacrificial layer,

Welbourn et al. discloses a method of using sacrificial layers S1 and S2, whereby a portion of the sacrificial layers is retained, an intervening layer is located between the sacrificial layer S2 and the substrate S, the sacrificial layer S2 is patterned, wherein removal of the sacrificial layer S2 removes a portion of the underlying sacrificial layer S1, and wherein through holes are opened to reach the sacrificial layer followed by the formation of additional layers to close the through holes (see figs. 1-12 and their description). In view of this disclosure, it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify the process of Steiner et al. so as to use the sacrificial layer process of Xiang-Zheng et al. so as to form a MEMS device because this is shown to be a suitable method in which to form a MEMS device.

Claims 67 and 97 are rejected under 35 U.S.C. 103(a) as being unpatentable over Xiang-Zheng et al., U.S. Patent 5,242,863 in view of Burns et al., U.S. Patent 6,048,734.

Xiang-Zheng et al. is applied as above but fails to expressly disclose adding liquid or gas into the cavity structure and using the cavity for movements of chemicals.

Burns et al. discloses adding Freon into a cavity prior to sealing (see col. 23-lines 10-45) and using the device for transportation of chemicals (see abstract). In view of this disclosure, it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify the process of Xiang-Zheng et al. so as to fill the cavity with liquid as shown by Burns et al. because this is shown to be an effective method to fill an airgap.

Claims 28 and 70-71 are rejected under 35 U.S.C. 103(a) as being unpatentable over Xiang-Zheng et al., U.S. Patent 5,242,863 or Steiner et al., "Using porous silicon as a sacrificial layer" or Tu et al., U.S. Patent 5,352,635.

The above references are applied as above but fail to show the height and width of the cavity structure. However, it would have been obvious to one of ordinary skill in the art at the time the invention was made to determine through routine experimentation the optimum height and width of the cavity based upon a variety of factors including the device dimensions and would not lend patentability to the instant application absent the showing of unexpected results. Regarding the use of a stencil layer, the examiner takes official notice that it is prima facie obvious to utilize stencil layers for the purposes of patterning layers.

Claim 19 is rejected under 35 U.S.C. 103(a) as being unpatentable over Xiang-Zheng et al., U.S. Patent 5,242,863 in view of Burns et al., U.S. Patent 6,048,734.

Xiang-Zheng et al. is applied as above but fails to expressly disclose forming through-holes through the substrate to remove the sacrificial layer.

Burns et al. discloses forming through holes 36 to remove the sacrificial material (see col. 23-lines 10-45). In view of this disclosure, it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify the process of Xiang-Zheng et al. so as to remove the sacrificial material using through holes in the substrate because such a method is a suitable way to remove sacrificial material.

Claims 19 and 23 are rejected under 35 U.S.C. 103(a) as being unpatentable over Yonehara et al., "ELTRAN; SOI-Epi Wafer by Epitaxial Layer Transfer from Porous Si" in view of Burns et al., U.S. Patent 6,048,734.

Yonehara et al. is applied as above but fails to expressly disclose forming through-holes through the substrate to remove the sacrificial layer.

Burns et al. discloses forming through holes 36 to remove the sacrificial material (see col. 23-lines 10-45). In view of this disclosure, it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify the process of Xiang-Zheng et al. so as to remove the sacrificial material using through holes in the substrate because such a method is a suitable way to remove sacrificial material.

Allowabl Subject Matter

Claims 29-33 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Claims 73-89 and 90-96 are allowed.

The following is a statement of reasons for the indication of allowable subject matter: the prior art, either singly or in combination, fails to anticipate or render obvious, the limitations of: the step of lifting off said stencil layer, thereby also removing a portion of said high surface area to volume ratio material layer deposited thereon, as required by dependent claim 29 and independent claim 73. Furthermore, the prior art also fails to suggest: removing a portion of said high surface area to volume ratio material layer to expose a portion of said first material system, and removing said high surface area to volume ratio material layer, thereby freeing a portion between said first and second material systems while maintaining at least one contact region, as required by independent claim 90.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Richard A. Booth whose telephone number is (571) 272-1668. The examiner can normally be reached on Monday-Thursday from 7:30-6:00.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, John Niebling can be reached on (571) 272-1679. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Richard A. Booth
Primary Examiner
Art Unit 2812

May 28, 2004